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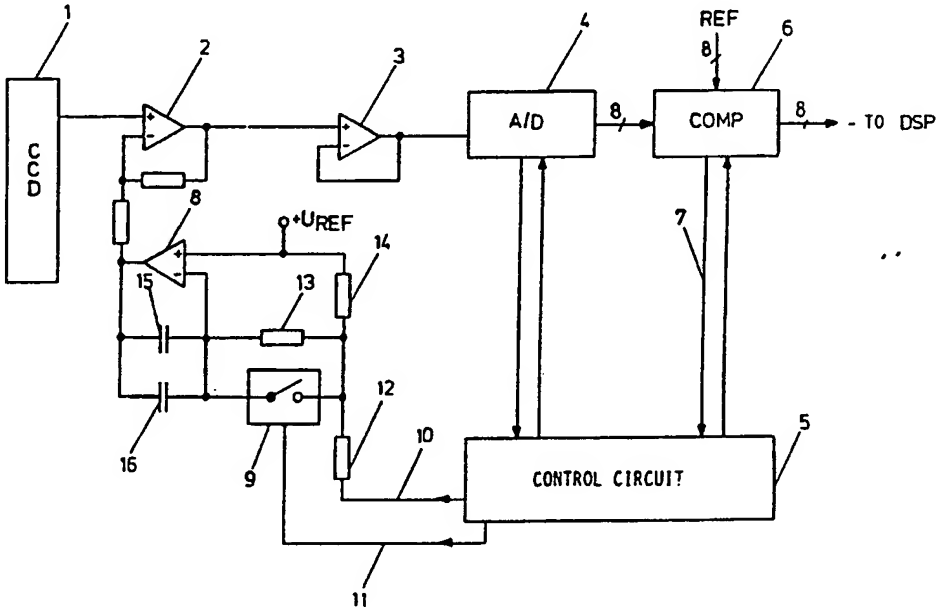
(54) Title: METHOD AND APPARATUS TO COMPENSATE FOR THE DARK CURRENT AND OFFSET VOLTAGE FROM A CCD-UNIT



(57) Abstract

The invention discloses a dark current compensation circuit for a CCD-unit. This dark current compensation circuit is characterized in that the dark current compensation is performed directly on the analog output signal from the CCD-unit the control loop comprising parts of the digital signal processing of the signals from the CCD-unit so as to further achieve a compensation for the temperature drift of said parts.

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Method and apparatus to compensate for the dark current and offset voltage from a CCD-unit.

The invention relates to a circuit for compensating for the dark current and thermal drift in the output voltage from a CCD-unit.

When using a CCD-unit for an image generating scanning it is generally known that it is necessary to compensate for the part of the output voltage originating from the dark current and thermal drift of the CCD-unit.

This compensation is usually effected either by compensating directly in the analog signal from the CCD-unit or by converting the analog signal into digital representations which are processed in a digital processing unit for that purpose.

Both of these compensating methods suffer, however, from certain shortcomings. By compensating only the analog signal no compensation is made for the drift of the subsequent A/D-converter, thereby causing an essential error from the temperature dependent offset voltage drift of this A/D-converter.

If a digital processing unit is used for the compensation, drift in all the units positioned ahead of the processing unit can be compensated for, but this compensation is very troublesome as to computation and thereby also time consuming. Moreover, it is necessary to use an A/D-converter with a very high resolution if the compensation shall be effected sufficiently accurately. Moreover, this A/D-converter shall be fast, implying that this component gets very expensive.

The purpose of the present invention is to provide a method and an apparatus by which it is possible to effect the desired dark current and offset voltage compensation in such a way that the A/D-converter is included in the compensation loop without basing the

compensation on computations in a digital processing unit and without using a high resolution A/D-converter.

This purpose is achieved by the method specified in the characterizing portion of claim 1. The use of this method allows for compensating for dark current variations in the CCD-unit and for compensating for all the temperature dependent variations of the output voltages and conditions of all elements in the circuit.

By using a circuit with two time constants as specified in the characterizing portion of claim 2 a quick tracking of the compensation circuit is obtained upon its activation.

Claims 4 and 5 indicate preferred embodiments of the invention, claim 5 particularly specifying how it is possible to use an A/D-converter for conversion and dark current compensation for line pulses from a CCD-unit with two outputs.

Claim 3 defines a particularly advantageous embodiment of the circuit, and it will be seen that only one single A/D-converter with a resolution corresponding to the wanted grey tone resolution is necessary.

The invention will now be described in more detail with reference to the drawings, in which

Fig. 1 shows a circuit in accordance with the invention, and

Fig. 2 shows a preferred embodiment of the invention.

Fig. 1 shows a circuit according to the invention. The purpose of the circuit is to convert analog signals from a CCD-unit 1 into digital representations.

The output signal from the CCD-unit 1 is fed to a first amplifier 2, from the output of which the signal is fed to another amplifier 3, the output signals of which is fed to an A/D-converter 4. The

A/D-converter is connected to a control logic circuit 5 and a digital comparator 6.

Control circuit 5 serves to control A/D-converter 4 and the comparator 6 and to supply, in dependence on the output 7 from comparator 6, control signals to an amplifier 8 and a switch 9 via lines 10 and 11.

CCD-unit 1 is of the type comprising a plurality of masked cells and the output voltage from these cells is used as a measure of the dark current in all of the cells of the CCD-unit. According to the invention the voltage level from the masked cells in CCD-unit 1 is read out, the signal voltage is amplified in amplifiers 2 and 3 and converted into digital representations in A/D-converter 2. The comparator compares said digital representations to a predetermined digital number and supplies the result of the comparison to the control logic.

If the comparator signal 7 indicates that the signal from the masked cells is too high, then the working point of amplifier 2 is shifted in a negative direction by supplying a positively moving signal from amplifier 8 to its negative input, said amplifier 8 constituting together with the resistors 12, 13, 14 and capacitors 15 and 16 an integrator whose time constant can be changed by switch 9. This integrator is arranged so that the direction of the voltage changes at the output is determined by the voltage level on line 10.

If the output signal from the A/D-converter is far from the optimum, switch 9 is closed, thereby materially reducing the time constant of the integrator. The time of activating switch 9 is controlled by control logic 5 controlling the switch via line 11. When the output signal from the A/D-converter approaches the optimum, switch 9 is reopened and the

integrator operates at a high time constant. This provides for obtaining a faster tracking.

When the output signal from the A/D-converter becomes too low, this is detected by control logic 5 inverting the voltage on line 10, following which the direction of the change of the output voltage from the integrator changes.

Under this control the output voltage of A/D-converter 4 always oscillates around the optimum value. The characteristic feature of the described control is that it includes almost all parts of the circuit whose drift may influence the output signal from A/D-converter 4. The control loop thus includes amplifiers 2 and 3, A/D-converter 4 and integrator 8. This makes it possible to compensate for changes in the output voltages of said components, said changes being mainly due to thermal variations.

Fig. 2 shows a preferred embodiment of the invention making use of a CCD-unit with two outputs. According to the invention the circuit associated with said CCD-unit is structured as shown in Fig. 2. The parts illustrated in Fig. 2 having the same function as in Fig. 1 are indicated by the same reference numerals. As it will appear, the circuit illustrated in Fig. 2 consists substantially of two sets of circuit elements identical with those shown in Fig. 1. An amplifier 2 or 2', an integrator 8 or 8' and a switch 9 or 9' are associated with each output from the CCD-unit. The output signals from amplifiers 2 and 2' are fed to switches 17 and 18. These switches provide for multiplexing the signal from amplifiers 2 and 2' to the input of amplifier 3.

The control loop is in this case composed of the same components as shown in Fig. 1, use being made, however, of a common A/D-converter 4 and a common comparator 6 for both outputs of the CCD-unit.

An optimum utilization of the most expensive components of the control loop is attained by the above structure of the control loop, i.e. A/D-converter 4 and comparator 6.

In the above explanation it has been presumed that the CCD-unit is of the linear type, i.e. composed of a plurality of light-sensitive elements positioned along a straight line. In this way each read-out from the CCD-unit yields a representation of a line in the image to be scanned. This, however, involves another problem in the dark current compensation, because the latter has to be kept constant for each line to be read out. This problem is solved according to the invention by giving the integrators in association with amplifiers 8 and 8' so high time constants that their output signal will be approximately constant during the time it takes to read out one line from the CCD-unit.

This high time constant of the integrators, however, causes the disadvantage that the tracking time of the control loop becomes very long. To obviate said disadvantage the integrators according to the invention are constructed to work at two time constants controlled by switches 9 and 9'. In a first position of the switches the integrators work at a low time constant used for tracking the control loop when is is far from the optimum dark current compensation, that is for instance the situation upon the starting-up of the apparatus or in case of big fluctations in the surrounding temperatures. In the second position of the switches the integrators work at a high time constant, thereby attaining the desired stable regulation around the optimum dark current compensation.

The above specified structure of the integrator actually provides for obtaining a quick tracking to the optimum compensation and a stable regulation around this optimum compensation, thereby preventing the dark

current compensation from changing during the read-out of one single line.

Control logic 5 is not discussed in detail here, this being a circuit of conventional type. In a preferred embodiment of the invention the control logic is constructed by means of a programmable logic network since it is then possible to implement the control logic in one single circuit.

In the preceding, the CCD-unit is regarded to be a separate unit capable of reading out its own signals. However, this is incidentally not the fact and in a practical embodiment of the invention it is necessary to provide the control signals necessary for the CCD-unit. When using a programmable logic network for the implementation of the control logic it is possible to implement the generation og said control signals in the control logic in a simple and economic manner.

PATENT CLAIMS

1. A method of compensating for the dark current and the offset voltage from a CCD-unit of the kind comprising a plurality of masked cells, the output voltage level from the masked cells being used as a measure of the dark current, characterized in

- that the output voltage from the masked cells is converted from analog into digital form,

- that the digital word representing the dark current is compared to a predetermined digital word, and

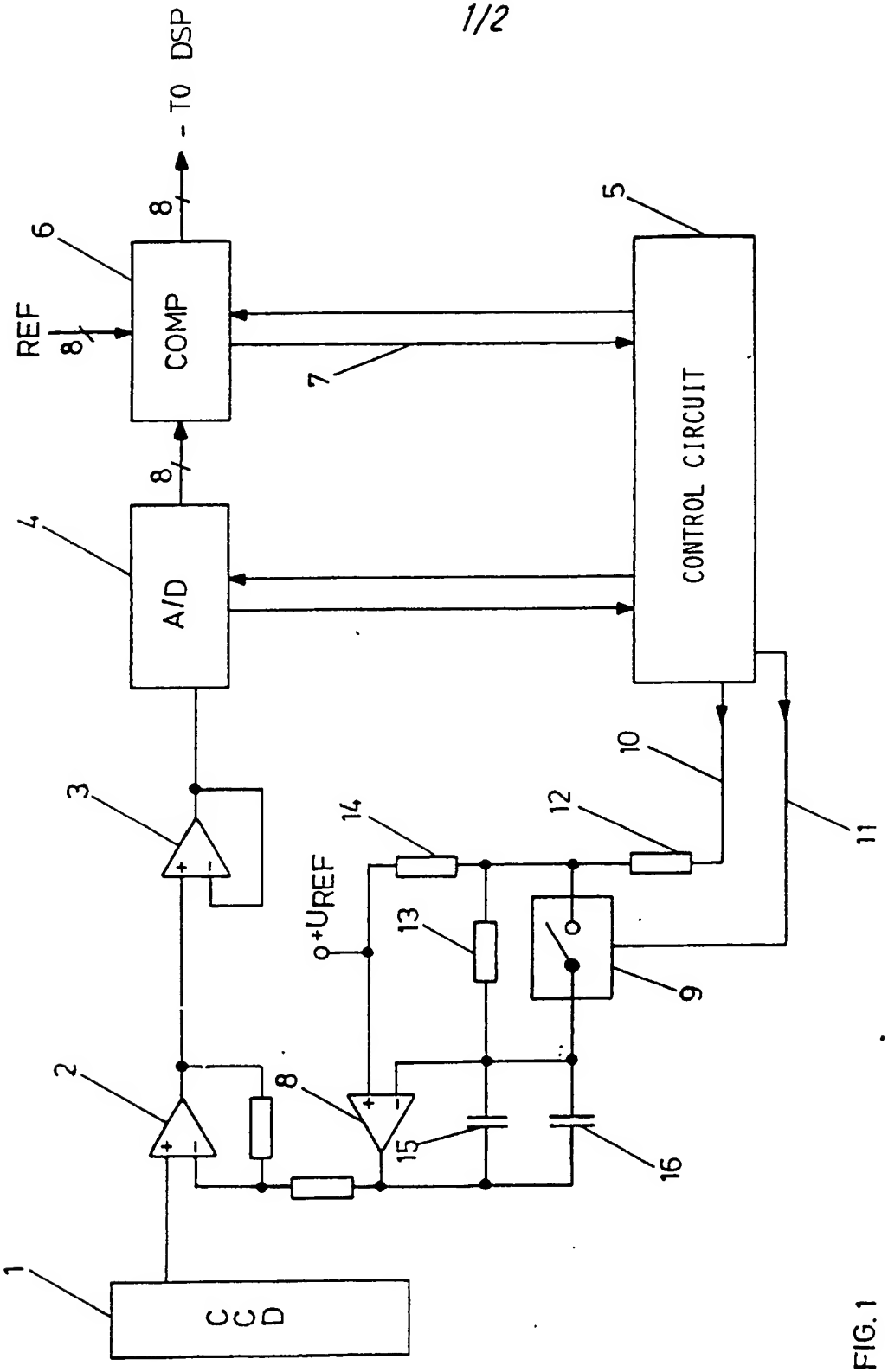
- that in dependence on the result of the comparison a shift of the offset voltage to an amplifier inserted in the signal path is effected until the digital word representing the dark current equals the predetermined word.

2. A method as claimed in claim 1, characterized in that a CCD-unit with two output signals is used and that the compensation for the dark current is performed alternately for each of the output signals.

3. An apparatus for carrying out the method according to claim 1, characterized in that it comprises a control loop composed of an amplifier (2), a buffer (3), and A/D-converter (4), a comparator (6), a control logic (5) and an integrator (8), the control logic being arranged to change the inclination of the ramp of the integrator in dependence on the signal from the comparator, and that the integrator (8) is intended to shift the zero point of the amplifier (2).

4. An apparatus as claimed in claim 3, characterized in that the integrator (8) is adapted to work at least at two different time constants.

5. An apparatus as claimed in claims 3 and 4, characterized in that switches (17 and 18) are inserted in front of the amplifier (3), said switches being controlled by the logic (5) and intended to multiplex signals from amplifiers (2 and 2').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COMP
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CONTROL CIRCUIT
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A/D
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11
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+UREF
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15
16
1
CCD

FIG. 1

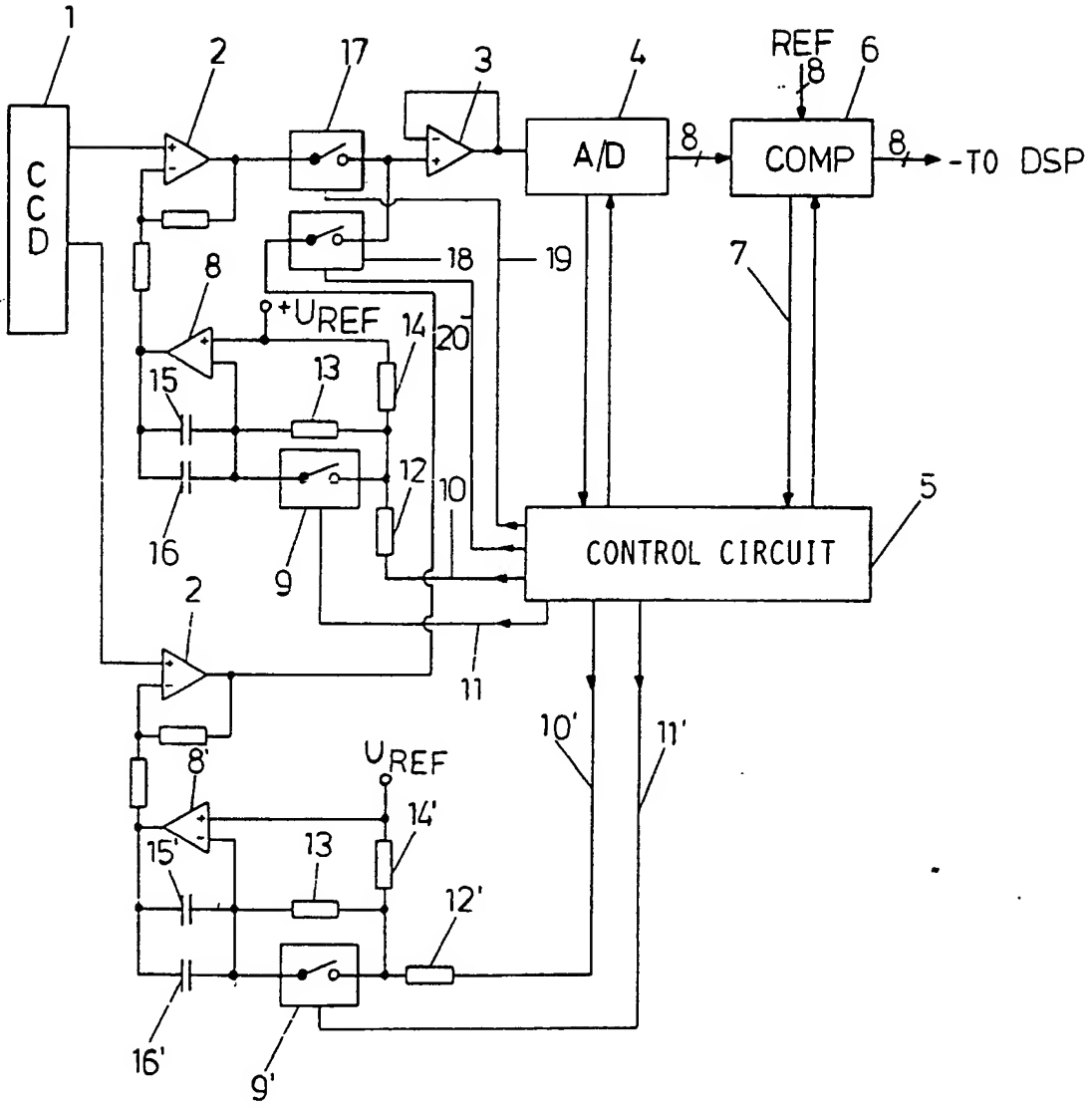
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FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No PCT/DK 89/00076

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC4: H 04 N 3/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System [7]	Classification Symbols
IPC4	H 04 N

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

SE, NO, DK, FI classes as above

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	DD, A1, 245047 (FRIEDRICH-SCHILLER-UNIVERSITÄT JENA) 22 April 1987, see abstract --	1
A	US, A, 4652927 (S. HASHIMOTO) 24 March 1987, see abstract; figure 4 --	1
A	US, A, 4473839 (M. NODA) 25 September 1984, see abstract --	1-5
A	US, A, 4580168 (P.A. LEVINE) 1 April 1986, see the whole document --	1-5
A	US, A, 4589025 (J.F. MONAHAN ET AL) 13 May 1986, see the whole document ---	1-5

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
1989-07-10	1989 -07- 17
International Searching Authority	**Signature of Authorized Officer**
Swedish Patent Office	Rune Bengtsson

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. PCT/DK 89/00076

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DD-A1- 245047	22/04/87	NONE	
US-A- 4652927	24/03/87	JP-A- 59100671	09/06/84
US-A- 4473839	25/09/84	JP-A- 58083488	19/05/83
		DE-A-C- 3242224	01/06/83
US-A- 4580168	01/04/86	JP-A- 58213572	12/12/83
		US-A- 4496982	29/01/85
US-A- 4589025	13/05/86	GB-A-B- 2168218	11/06/86
		FR-A- 2574241	06/06/86
		DE-A- 3542101	05/06/86
		JP-A- 61133784	21/06/86